EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	101	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) near3 (trac$3 track$3) with channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 07:56
L6	7	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) near3 (trac$3 track$3) with channel and (pattern model$3 template) near3 (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 08:34
L7	21	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) with (trac$3 track$3) with channel and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 09:06

L9	113	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) with (trac$3 track$3) and (pattern model$3 template) with channel and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 09:15
L10	53	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) near5 (trac$3 track$3) and (pattern model$3 template) near5 channel and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 09:16
L11	6	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) with (trac$3 track$3) and (pattern model$3 template) with channel and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3) and ("716"/$.ccls. "257"/$.ccls. "438"/$.ccls. "430"/$.ccls. "361"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 09:24

L17	10	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3) and channel with (trace track $3) and ("716"/$.ccls. "257"/$.ccls. "438"/$.ccls. "430"/$.ccls. "361"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 10:53
L18	16	(pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) with (fpga or pld cpld or (programmable adj device) asic device circuit $2) and (pattern model$3 template) with (trac$3 track$3) with (optim$5 refin$3 modif$3 chang$3 rewir$3 rerout$3 configur $3) and channel with (trace track$3) and ("716"/ $.ccls. "257"/$.ccls. "438"/ $.ccls. "430"/$.ccls. "361"/ $.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/26 10:57
S16	31	((pld or fpga or cpld) near3 (component or cell or element or device or asic)) same (contact$3 or conduct$3 or lead$3 or connect$3 or interconnect $3) same ("i/o" or (input adj output) or pin or ball or column) same (assign $5 or map$4) and ("716"/ $ "174"/$ "29"/$).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 11:32

S18	23	((pld or fpga or cpld) near3 (component or cell or element or device or asic)) same (contact$3 or conduct$3 or lead$3 or connect$3 or interconnect $3) same ("i/o" or (input adj output) or pin or ball or column) same (assign $5 or map$4) and (optimiz $4 or improv$3) and ("716"/$ "174"/$ "29"/$). ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 11:33
S228	4	nortel adj network.as. and (assign$5 map$4 select$3 allocat$3 indicat$3 identif $3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern and trace and channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/18 13:06
S231	4	(fpga or pld cpld or (programmable adj device)) same (map$4 connect$3 interconnect$3 wiring coupl$3) same ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$5 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern same trace and (channel same (rout $3 interconnect$3 connect $3 wiring)) and @pd<"20000619"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/24 16:06

S235	44	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$5 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern same trace and (channel same (rout $3 interconnect$3 connect $3 wiring)) and (via hole)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/24 19:03
S237	39	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$6 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern same trace and (channel same (rout $3 interconnect$3 connect $3 wiring)) and (via hole) and layer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/24 19:05

S239	77	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$6 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern same trac$3 and (channel same (rout $3 interconnect$3 connect $3 wiring)) and (via hole) and layer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 09:37
S244	5	muff.in. and chip and ic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 11:04
S247	71	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3 oriogram$4 configur$5) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$6 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern and trace and (channel same (rout$3 interconnect$3 connect$3 wiring)) and (via hole) and layer and mirror$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 15:05

S248	11	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3 oriogram$4 configur$5) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$6 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and pattern same trace and (channel same (rout $3 interconnect$3 connect $3 wiring)) and (via hole) and layer and mirror$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 15:06
S250	4	(fpga or pld cpld or (programmable adj device)) with (map$4 connect$3 interconnect$3 wiring coupl$3 oriogram$4 configur$5) with ((electronic adj device) device circuit$2 (electronic adj component) asic processor microprocessor macro$4 fpga or pld cpld or (programmable adj device)) and (assign$6 map$4 select$3 allocat$3 indicat$3 identif$3 determin$3 prescrib$3 specif$3 designat$3) with (contact pin ball column) and (trace track$3) with channel with via and pattern with (trace track $3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 15:53

S255	8	channel same (via hole) same layer and (pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) same (fpga or pld cpld or (programmable adj device)) same (map$4 connect$3 interconnect$3 wiring coupl$3) and pin with (assign$4 allocat$3 select$3 plac$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 16:08
S256	62	channel same (via hole) same layer and (pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) same (fpga or pld cpld or (programmable adj device)) same (map$4 connect$3 interconnect$3 wiring coupl$3) and (contact pin ball column) with (assign$4 allocat$3 select$3 plac$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 16:18
S262	5	channel same (via hole) same layer and (pcb pwb (circuit adj board) (printed adj board) (wiring adj board) board) same (fpga or pld cpld or (programmable adj device)) and (pattern model$3 template) with (trac$3 track$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/25 18:08

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